IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC 2025)

October 12-15, 2025
Puerto Varas, Chile

Program at a Glance

	12 - oct. - 25				13 - oct. - 25		14 - oct. - 25		15 - oct. - 25	
08:30	Registration			08:30	Opening					
09:00	Tutoria 1	Tutorial 2		09:00	Session 1	Session 2	Session 3	Session 4	Session 5	
09:30				09:30						
10:00				10:00						
10:30	Coffee break			10:40	Coffee break		Coffee break		Coffee break	
11:00	Tutorial 1	Tutorial 2		11:10	Keynote 1		Keynote 2		Keynote 3	
11:30				11:30						
12:00				12:10	Lunch		Lunch		Lunch	
12:30				12:30						
13:00	Lunch			13:00						
13:30				13:30						
14:00				14:00	Special session		Social event		Special session	
14:30	Tutorial 1	Tutorial 2		14:30						
15:00				15:00					Session 6	
15:30				15:20	PhD Forum					
16:00	Coffee break			15:40	Coffee break and posters					
16:30	Tutorial 2	Tutorial 2		16:00						
17:00				16:20	Panel				Closing ceremony	
17:30				17:00						
18:00				17:30						
18:30	Welcome reception			18:00					Farewell party	
19:00				18:30						
19:30				19:00						
20:00				19:30			Gala dinner			
20:30				20:00						
21:00				20:30						
21:30				21:00						

Sunday October 12th, 2025

Tutorial 1, 9:00 – 18:00: "Power Analysis Optimizations – Fundamentals to Advanced Implementations" , Ronald Valenzuela and Benjamin Villegas (Synopsys, Chile)

Tutorial 2, 9:00 – 18:00: "Integrated circuits design using IHP SG13G2 open-source PDK exploring local and cloud-based design environments" , Juan Sebastian Moya-Baquero (Symbiotic EDA, Colombia), Jorge Marin (AC3E/USM, Chile), and Krzysztof Herman (IHP, Germany).

Monday October 13th, 2025

Session 1: EDA (9:00 – 10:40)

"Delay Mismatch Optimization in Routing Dominated Multi-Path Systems: A Case Study on an IR-UWB Edge-Combiner Transmitter Front End#, Kyla Marie Juruena, Maria Ena Rosales, Trisha Renee Capulong and Louis Alarcon

"Inter-chip Clock Network Synthesis on Passive Interposer of 2.5D Chiplet Considering Tran", Tai Yan, Yiyu Wang, Zhan Li, Ning Xu and Yuanqing Cheng

"Automated Generation of Microfluidic Netlists using Large Language Models", Jasper Davidson, Skylar Stockham, Allen Boston, Ashton Snelgrove, Valerio Tenace and Pierre- Emmanuel Gaillardon

"Swift Synthesis of Approximate Hardware Accelerators Using Generative Adversarial Networks", Muhammad Awais, Hassan Ghasemzadeh Mohammadi and Marco Platzner

"Lightweight Congruence Profiling for Early Design Exploration of Heterogeneous FPGAs", Allen Boston, Biruk Seyoum, Luca Carloni and Pierre-Emmanuel Gaillardon

Session 2: Digital Design 1 (9:00 – 10:40)

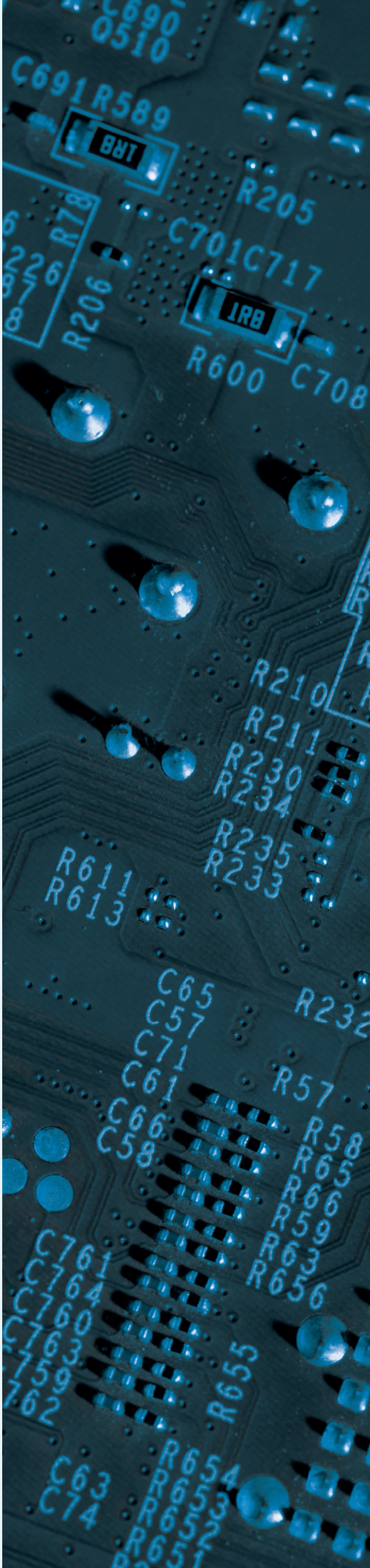
"On the Possibility of Relying Solely on FeMFET Variability for PUF Implementations", Miqueas Filsinger, Antoine Cauquil, Damien Deleruyelle, David Navarro, Ian O'Connor and Cédric Marchand

"Toward Multi-Person Breath Rate Estimation via mmWave Radar", Cristian Turetta, Christian Farina, Chiara Bozzini, Morteza Varasteh and Graziano Pravadelli

"TSPC-Based Low-Power High-Resolution CMOS Phase Frequency Detector", Dhandeep Challagundla, Venkata Krishna Vamsi Sundarapu, Ignatius Bezzam and Riadul Islam

"LiC: Low-Cost Cache Replacement Algorithm for All Cache Levels", Varun Venkitaraman, Tejeshwar Thorawade, Mitul Tandon, Keerthisagar Kokkiligadda, Virendra Singh and Janak Patel

"Energy-Ekicient Computation of TensorFloat32 Numbers on an FP32 Multiplier", Per Larsson-Edefors



Keynote (11:10 – 12:10)

"Multi-Die Design and Integration", Brandon Wang

Special Session 2: Open Source Silicon (14:00 – 15:20)

"Open-Source Approach to IC Development: Validation Against Measurements of Selected Devices from the IHP-Open-PDK", Krzysztof Herman and Dietmar Warning

"Open-Source 4 K CMOS Calibration: Integrating IceMOS and Sky130 PDK", Mauricio Montanares, V.H. Arzate Palma, Kevin G. McCarthy and Gerardo Molina Salgado

"PVT-Robust Analog Control Stage for Buck DC-DC Converters in Open-Source SKY130", Juan Pablo Martinez Brito, Jorge Marin, Giordano Rossa, Henrique Beque and Iuri Tinti

"Implementation of a 16:1 Multiplexer and 1:16 Demultiplexer on a Single Chip Using Sky130 PDK and Open-Source EDA Tools for Silicluster", Uriel Jaramillo Toral, Susana Ortega Cisneros, Emilio Isaac Baungarten Leon, Erick Jaramillo Toral and Hector Emmanuel Muñoz Zapata

PhD and Student Forum (15:20 – 16:20)

PhD Forum

"Agentic AI for Hardware Design Language: An Autonomous Pipeline for Verilog Code Generation, Simulation, Verification and Analysis"
, Ashutosh Singh, Kunal Iiitd and Anuj Grover

"Hybrid Lightweight Soft Error Mitigation Techniques for Edge Devices"
, Jonas Gava, Ricardo Reis and Luciano Ost

"Cross-Layer Approximate Hardware Design of Interpolation Filters for Fractional Motion Estimation in Versatile Video Coding", Rafael da Silva, Mateus Grellert and Ricardo Reis

Student Forum

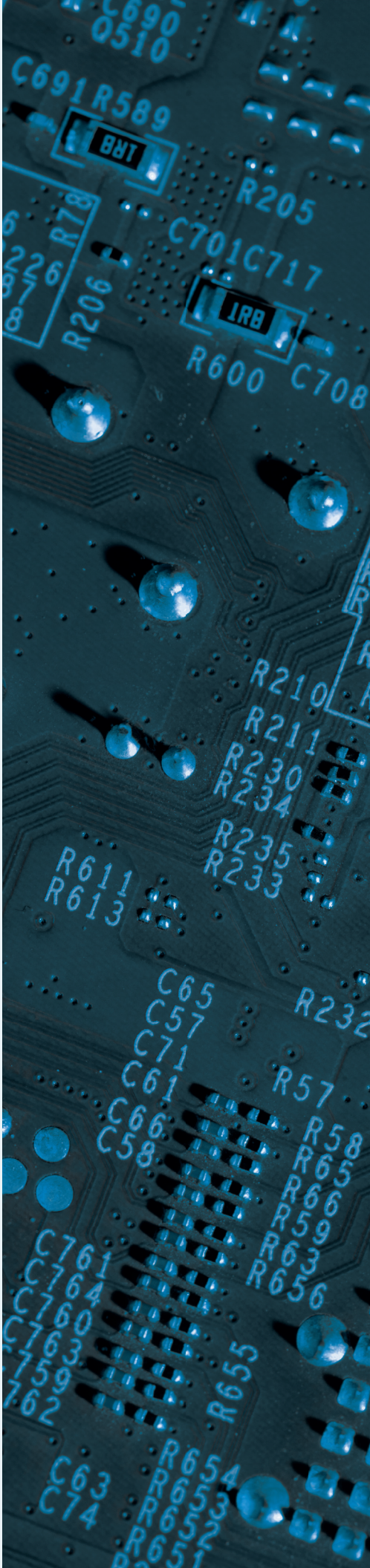
"Towards Full Integration of a Three-Level Flying Capacitor Converter Control in a Mixed-Signal ASIC", Nelson Salvador, Francisca Donoso, Jorge Marín, Victor Grimblatt and Christian Rojas

"Design of a 32nm Ultra-Low Power 6T SRAM Cell Analyzing Modern Technologies such as FinFET, TFET, and CNFET for energy-ekicient applications", Jesus Gonzalez

"A Novel CMOS Time Register", Johnatan Felipe, Dalton Colombo, Kamal El-Sankary and Mahsa Zareie

"A Case Study on the Migration of a High-Level PI Controller to ASIC-Compatible HDL Representation", Francisca Donoso, Nelson Salvador, Jorge Marín, Christian Rojas and Gonzalo Carvajal

"Transistor Placement for Automatic Cell Layout Generation on Advanced Nodes: A Review", Vitor Hugo Fuerstenau and Ricardo Reis



Tuesday October 14th, 2025

Session 3: Design for AI hardware and emerging applications (9:00 –10:40)

“From Secure Storage to Compute-in-Memory: A Versatile Memory System using 1T-nC FeRAM”, Rakesh Acharya, Rudra Biswas, Jiahui Duan, Prapti Panigrahi, Kai Ni and Vijaykrishnan Narayanan

“Non-volatile Ferroelectric-AND (FeAND) memory cell design”, Basile Darne, Miqueas Filsinger, Alberto Bosio, Damien Deleruyelle, Ian O'Connor, Bertrand Vilquin and Cédric Marchand

“Accelerating Machine Learning using RISC-V Vector Extension in a Manycore Platform”, Willian Analdo Nunes, Antônio Santos, César Marcom and Fernando Gehm Moraes

“Conjunctive Merge Instruction to Accelerate Sparse Matrix - Dense Vector Multiplication”, Manuel Osterno, César Marcon, Jarbas Silveira, Fernando Moraes and Jardel Silveira

“Deus Ex LLMs: AI vs Humans in Post-Quantum Cryptographic Hardware Code Generation”, Ethan Cornett, Rahul Magesh, Sharath Pendyala, Elif Bilge Kavun and Aydin Aysu

Session 4: Reliability, Security and Fault Tolerance (9:00 – 10:40)

“TLGLock: A New Approach in Logic Locking Using Key-Driven Charge Recycling in Threshold Logic Gates”, Abdullah Sahruri and Martin Margala

“Trojan Attacks on Graph Convolution Neural Networks for Circuit Analysis”, Rupesh Raj Karn and Ozgur Sinanoglu

“Fault Modeling and Testing of Spin-Orbit Torque-Based Multipillar Memory Cell”, Arshid Nisar Laway, Lorena Anghel and Gregory Di Pendina

“Cultivating Security: Debug Authentication for Ensuring the Security of SoC's Root of Trust”, Arash Vafaei, Sujan Kumar Saha, Mark Tehranipoor and Farimah Farahmandi

“Application and Detection of Hardware Trojans Applied to Valid Data States of NCL Combinational Circuits”, Joao Pedro Magalhaes, Tales Pimenta and Diogo Leonardo Silva

Keynote (11: 10 – 12:10)

“Understanding the brain, from the perspective of EE”, Lou Scheker

Social Event (14:00 – 19:00)

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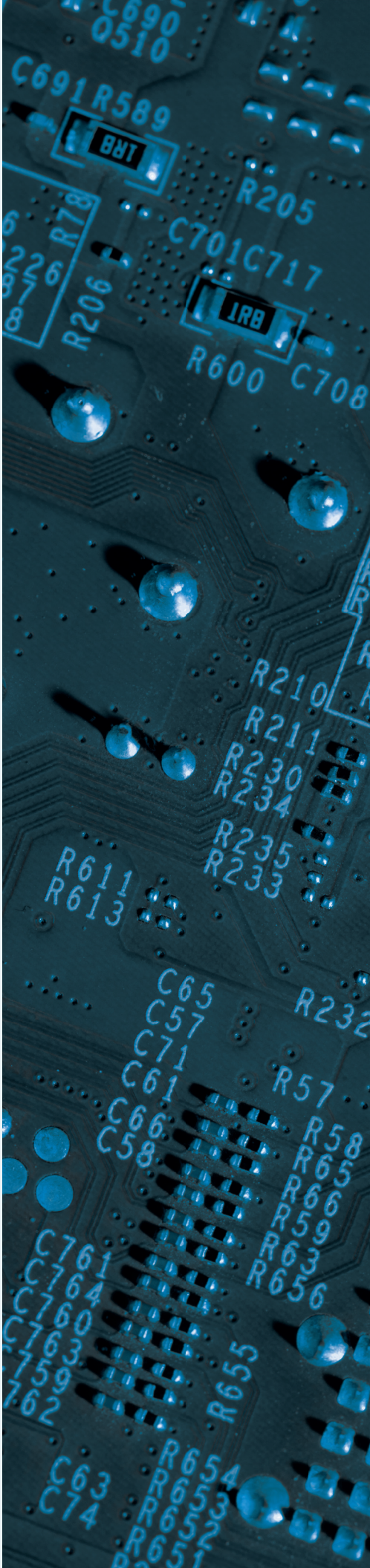
Gala Dinner (19:00 – 22:00)

https://asic-chile.cl/vlsisoc/social-event/



Wednesday October 15th, 2025

Session 5: EDA (9:00 – 10:40)

"Mission Profile-Driven Transistor Aging Modeling and Simulation Flow", Firas Ramadan, Maayan Ella and Freddy Gabbay

"Exploring Enhancements of 1T1C FeMFET Bitcell With a Versatile DTCO Methodology", Rosario Pronsato, Antoine Cauquil, Pascal Vivet, Jean Coignus, Damien Deleruyelle, Cédric Marchand, Alberto Bosio, Lioua Labrak and Ian O'Connor

"ML4FPGA: An LLM Framework for Electronic Design Automation and Verification on FPGA", Leo Udeji and Martin Margala

"EmFIA: A Novel Emulation-based Fault Injection Vulnerability Assessment Framework at RTL Level", Tanvir Rahman, Shuvagata Saha, Sujan Kumar Saha, Farimah Farahmandi and Mark Tehranipoor

"Noise and Quantization Parameterization of Photonic Convolution Accelerator", Mateus Vidaletti Costa, Mauricio Gomes de Queiroz, Raphael Cardoso, Ian O'Connor and Arnan Mitchell

Keynote (11:10 – 12:10)

"Cryogenic CMOS design techniques for scaled quantum computing systems", Sudipto Chakraborty

Special session 1: Novel hardware for Emerging Technologies and AI (14:00 – 15:00)

"Exploring MRAM for On-Chip Texture Storage in Rendering Applications", Nicolás Villegas, Stefano Romanini, Moritz Scherer, Warren Hunt, Syed Shakib Sarwar, Barbara De Salvo, Chiao Liu, Francesco Conti, Davide Rossi, Luca Benini and Jorge Gómez

"Scalability analysis of multi-bank near-memory computing in low-power SoCs", Luigi Giuffrida, Pasquale Davide Schiavone, Michele Caon, Guido Masera, Maurizio Martina and David Atienza

"Work in Progress: Exploring Silicon-Compatible Ferroelectric Oscillators for NP-Hard Problem Solving", Joaquín Welch, Jorge Gómez and Jaime Cisternas

Session 6: Digital Circuits 2

"Correlation Between Process Variability and Radiation Hardness in Digital Circuits", Elias de Almeida Ramos, Augusto Gouvêa Weber, Wilian Padilha, Renan Carlos Gomes de Farias, Joao Baptista Martins and Ricardo Reis

"Marker-Based Recognition for Autonomous Micro-Drone Flight: An FPGA-Optimized Feasibility Study", Diego Marcelo Ramírez Jove, Keisuke Sugiura and Yoshiki Yamaguchi,

"CMOS Time Register With High Dynamic Range", Johnatan Garcia, Dalton Colombo, Kamal El-Sankary and Mahsa Zareie

"A Low-Power 4-bit Tracking-Type Analog-to-Digital Converter in SKY130 Process", Esteban Astudillo, Eduardo Holguín, Esteban Garzón and Luis Miguel Prócel